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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/312,302	05/14/1999	MARIO D. NEMIROVSKY	P3803	2422

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EXAMINER
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DONAGHUE, LARRY D

ART UNIT	PAPER NUMBER
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2154

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DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/312,302

Applicant(s)

NEMIROVSKY ET AL.

Examiner

Larry D Donaghue

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 29 January 2003.  
2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-42 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date No. 12 10/21/03  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_

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1. Claims 1-42 are presented for examination.
2. The rejection is maintained and set forth below.
3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34, and 36-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemirovsky (DISC, A Dynamic Stream Computer).

Nemirovsky taught the invention as claimed including a processor executing a plurality of streams (page 63), a set of functional resources page (101 and 102) , interrupt logic (page 96) and interrupts are directed to one or more specific streams (page 63).

As to claim 2 and 3, Nemirovsky taught one exception or interrupt directed to two or more streams ( page 63) and two or more interrupts or exceptions are directed to one stream ( page 63).

As to claim 5, Nemirovsky taught that the directing is programmable (pages 94-98).

As to claim 6, Nemirovsky taught the interrupt logic refers to a data store (page 96, fig. 5.13).

As to claim 8 and 9, Nemirovsky taught the interrupts are from an external device and software interrupts (page 95).

As to claim 10, Nemirovsky taught a mask (page 96).

As to claims 11-12 , Nemirovsky taught after interrupting the streams and vectoring to a service routine (pages 96-97).

Claims 15-17, 19-20, 22-26, 29-31, 33-34, and 36-40 fail to teach or define above or beyond claims 1-3, 5-6, 8-12, and are rejected for the reasons set forth above.

5. Claims 4, 13-14, 18, 27-28, 32 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky as applied to claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34, and 36-40 above, and further in view of Nemirovsky et al. (DISC, A Dynamic Stream Computer).

Nemirovsky et al. (DISC, A Dynamic Stream Computer) reference was cited by applicant on paper no.2.

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As to claims 13, 27 and 41, Nemirovsky did not expressly teach delaying the vectoring to a service routine, Nemirovsky et al. taught that this technique is useful in synchronization (page 167, section titled Interrupts). It would have been obvious to one of ordinary skill in the art to combine these references as they are directed to the same device.

As to claims 14, 28, and 42, Nemirovsky taught that different streams vector to different service routines (page 96, first paragraph).

As to claims 4, 18 and 32, Nemirovsky (page 64) directing is static at processor design, by suggesting it would be beneficial to have a dedicated IS for interrupts.

6. Claims 7, 21 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky as applied to claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34, and 36-40 above, and further in view of applicant's admission.

The applicant's admission on paper no. 8, last paragraph of page 8 continued on to page 9, set forth that conditional and dynamic mapping is well-known in the art. It would be obvious to one of ordinary skill in the art to substitute one well known method of interrupt assignment for another to achieve the optimal desired performance.

7. Applicant's arguments filed 01/29/04 have been fully considered but they are not persuasive.

8. Applicant argues "Applicant argues the DISC computing system of Nemirovsky is extremely limited by the "pipeline" type instruction stream layering which makes it virtually impossible for instruction streams to truly simultaneously process instruction. Nemirovsky teaches a DISC (page 36). As explained in Nemirovsky, an important feature of DISC is that the instruction stream partition dynamically changes to optimize the processor utilization. Applicant points out that DISC utilizes pipelining in which multiple instructions from a (that is ...one) sequential instruction stream are simultaneously executed in an overlapped fashion. Nemirovsky teaches that a pipeline is compared to an assembly line in that the instruction is divided into multiple steps, the steps are called pipe stages. The stages are connected in a line, one next to the other, to form a pipe. Then an instruction is introduced at every single cycle at one end of the pipe while another exits the pipeline at the other end. Nemirovsky teaches that each stage of the pipeline processes a different piece of instruction simultaneously. Applicant argues that this pipeline system is one instruction stream divided into 4 separate sub-streams segmented into steps in a pipeline. Surely the Examiner can understand how this pipeline system fails to read on a plurality of physical hardware streams in a multi-streaming processor, as claimed.

9. The section referred to by applicant is the background of pipelining, Nemirovsky's adaptation of the pipeline begins on page 41, (section titled interleaving).

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10. Applicant further argues that the type of pipeline for an instruction stream as disclosed could not accommodate a flexible, dynamic mapping of interrupts and streams as claimed. As shown in Fig. 5.12, showing the sequencer of DISC architecture, streams and interrupts are assigned prior to streams actually detecting any interrupts. Clearly, Nemirovsky teaches away from applicant's invention as claimed.

11. The arguments of counsel cannot take the place of evidence in the record (145 USPQ 716, 718(CCPA)).

"Regarding the Examiner's 112 rejection of applicant's claims 7, 21, and 35, the Examiner stated that the claims contain subject matter which was not adequately described in the specification, and that applicant has merely supplied a suggestion to do. In the previous response applicant respectfully pointed out to the Examiner that conditional and dynamic mapping, as recited in the claims, is but one of several possible mechanisms used for processing external interrupts once an external interrupt has been detected. The interrupt logic receives the interrupt and decides which stream or streams to interrupt depending on the type of interrupt and on one or any combination of said mechanisms. Applicant is perplexed by the Examiner's insistence that further detail be given for conditional and dynamic mapping, which is but one of several such known mechanisms described in applicant's specification. For example, static mapping of interrupts, and programmable mapping of interrupts and exceptions are two other well-known mapping mechanisms which are described in applicant's specification, and are also recited in applicant's claims. " (emphasis added)

Clearly, applicant makes no such statement that dynamic mapping is well known in the art. Applicant only refers to dynamic mapping as known in applicant's specification.

12. Something can not be well known if only know at the time of filing, from the instant application.

13. Further, applicant believes that if the Examiner were to accurately use "Applicant's own admission" as an aid in a rejection it should come directly from applicant's specification, not an argument in a Response provided by applicant. Therefore, the Examiner's rejection of claims 7, 21 and 35 is certainly in error.

14. Attorney argument is not evidence unless it is admission, in which case, an examiner may use the admission in making a rejection. See MPEP 2145.

15. This is a RCE of applicant's earlier Application No. 09/312,302. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larry D Donaghue whose telephone number is 703-305-9675. The examiner can normally be reached on M-F 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 703-305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LARRY D. DONAGHUE  
PRIMARY EXAMINER

